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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/052,063

01/16/2002

Jonathon Cheah

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7590

06/04/2004

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SUITE 600

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EXAMINER

TU, CHRISTINE TRINH LE

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 06/04/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/052,063

Applicant(s)

CHEAH ET AL.

Examiner

Christine T. Tu

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 9, 12, 14-15 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9:

The phrase "the test pad is attached to the surface of the substrate on which are placed a plurality of electrical components" cannot be understood. It is not clear what is the test pad being done with the plurality of the electrical components.

Claim 12:

A method claim (Claim 12) cannot depend on an apparatus claim (claim 8).

Claims 14, 17, 18:

The term "the circuit" lacks antecedent basis. It is not clear where the circuit comes from.

Claims 15 and 19:

These claims are rejected because they depend on claims 14 and 17 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts et al. (5,734,661 and Roberts hereinafter).

Claim 1, 2, 9-10, 13-14, 16-18:

Roberts discloses the invention substantially as claimed. Roberts shows a method and apparatus for obtaining access to internal test circuits in integrated circuits being mounted on an integrated circuit die. Roberts shows (figure 4) that an integrated circuit die (38) includes one or more test circuit(s) (44), one or more bonding pad(s) (50) a switch circuit (48), and combination of a switch controller (54) and function circuit (40). The switch circuit (48) is connected through N lines to N respective bonding pads (50). The switch circuit (48) is controlled by the switch controller (54) to selectively connect the M lines of the test circuits (44) (figure 4, column 4 lines 5-37).

Robert does not explicitly teach the logic block. Robert, however, teaches the combination of the switch controller (54) and function circuit (40). It would have been

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obvious to one skilled in the art at the time the invention was made to name the combination of Robert's switch controller (54) and Robert's function circuit (40) (figure 4) as a "logic block". One having ordinary skill in the art would be motivated to do so because name such elements would not affect the performance of Robert's switch controller (54) and Robert's function circuit (40).

Claims 3-7:

Roberts teaches that the switch controller (100) uses a logic and a sequence decoder (120) and address decoder (122) for NAND gates for generating test signals (column 7 lines 1-51).

Claim 8:

Robert also shows a processor (210) is connected to bonding pads (220) for perform desired calculation and tasks (column 7 lines 55-60).


Claims 11-12, 15 and 19:

Robert teaches that as the switch controller (54) receives signals from a DRAM (as a functional circuit (40)), bonding pads (50) are connected to the test circuits (44) through the switch circuit (48) to allow tests to be conducted to determine the quality of the manufacturing process (column 5 lines 38-56).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Christine T. Tu
Primary Examiner
Art Unit 2133

May 29, 2004